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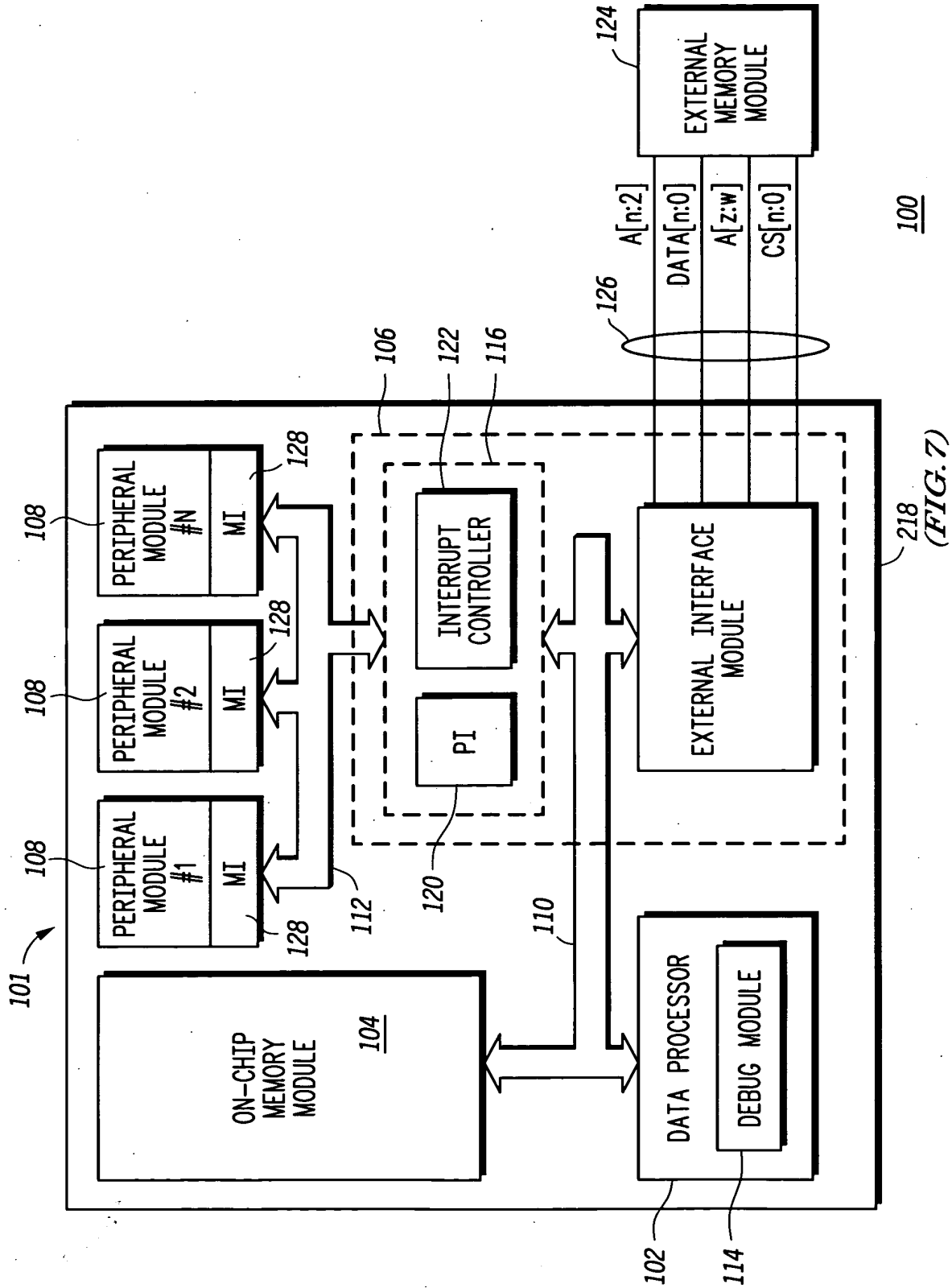


FIG. 1

DSZ BITS	PORT SIZE	PORT LOCATION	A[z]	A[y]	A[x]	A[w]
000	8 BIT	D[31:24]	A[n+1]	A[1]	A[0]	$\overline{EB[0]}$
001	8 BIT	D[23:16]	A[n+1]	A[1]	$\overline{EB[1]}$	A[0]
010	8 BIT	D[15:8]	A[n+1]	$\overline{EB[2]}$	A[1]	A[0]
011	8 BIT	D[7:0]	$\overline{EB[3]}$	A[n+1]	A[1]	A[0]
100	16 BIT	D[31:16]	A[n+1]	A[1]	$\overline{EB[1]}$	$\overline{EB[0]}$
101	16 BIT	D[15:0]	$\overline{EB[3]}$	$\overline{EB[2]}$	A[n+1]	A[1]
110	32 BIT	D[31:0]	$\overline{EB[3]}$	$\overline{EB[2]}$	$\overline{EB[1]}$	$\overline{EB[0]}$
111	32 BIT	D[31:0]	$\overline{EB[3]}$	$\overline{EB[2]}$	$\overline{EB[1]}$	$\overline{EB[0]}$

FIG.2

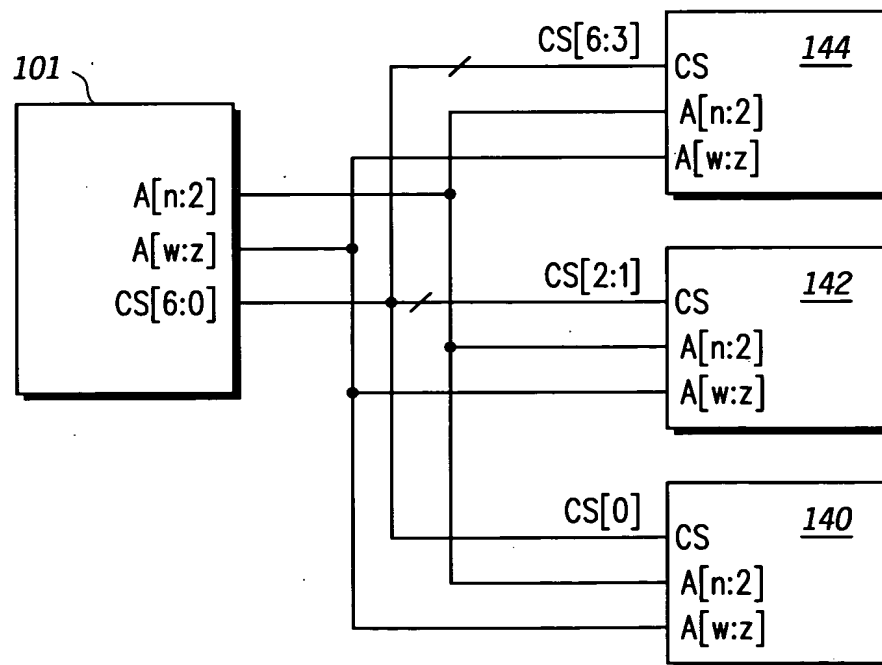


FIG.3

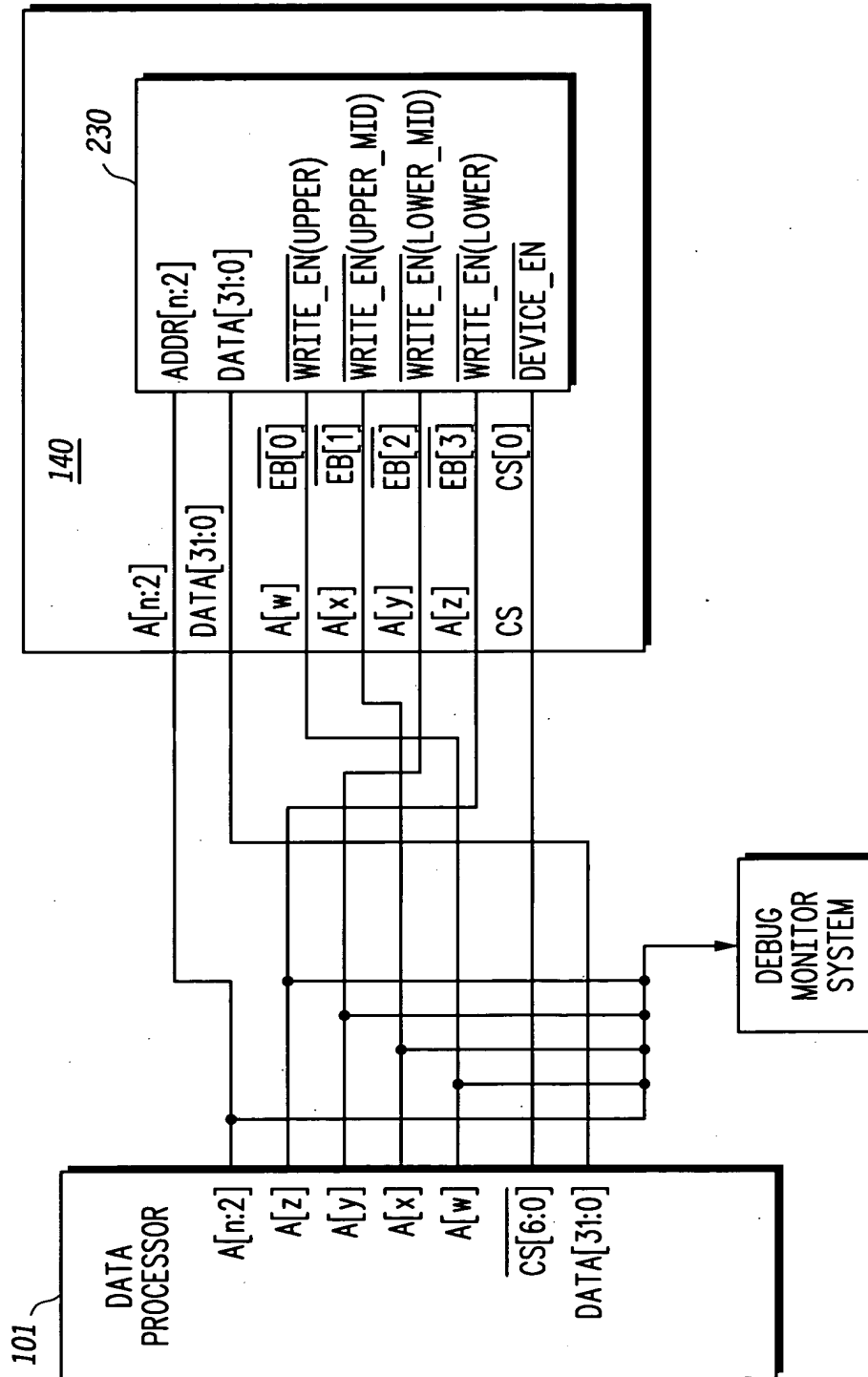


FIG. 4

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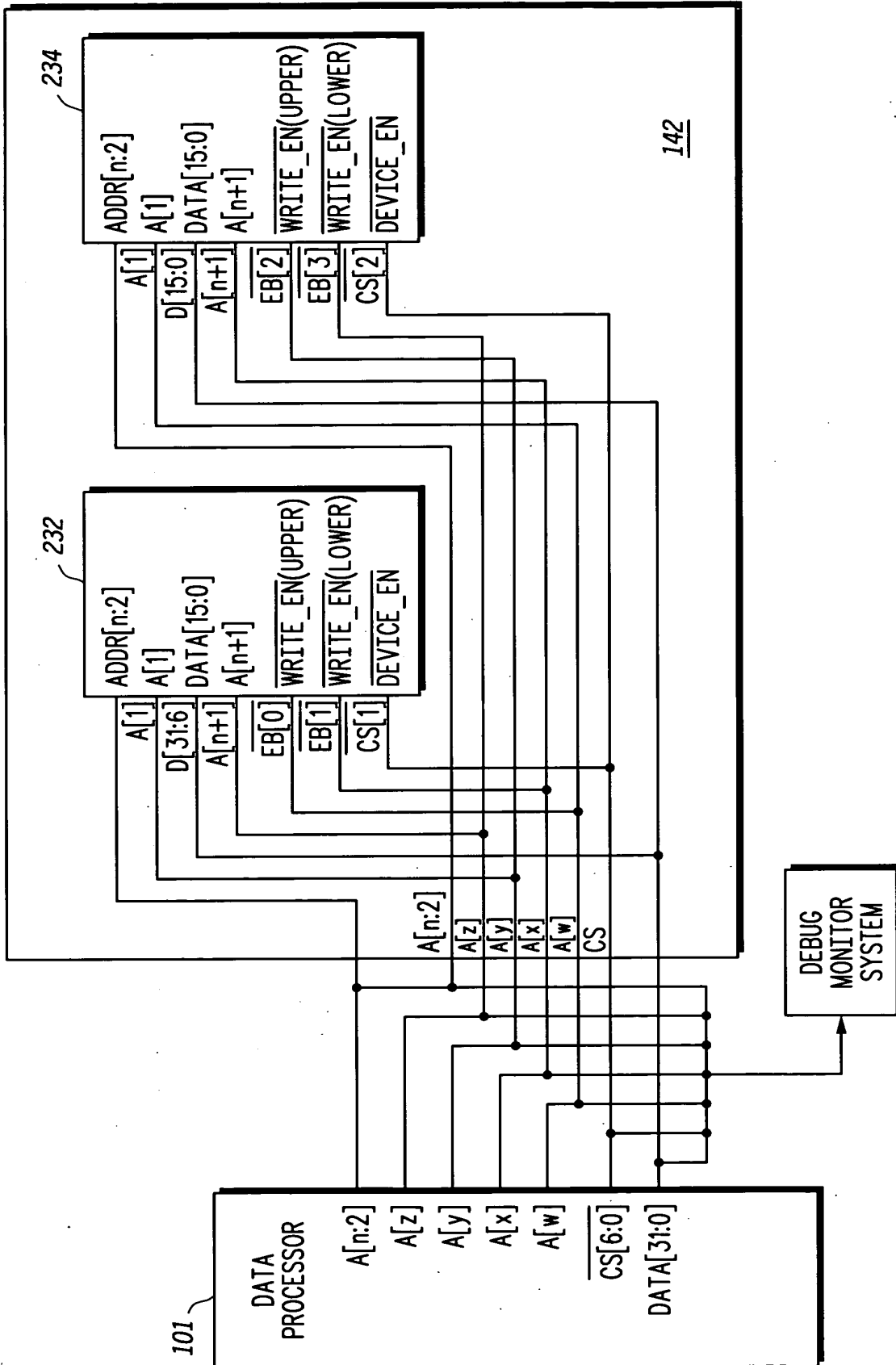


FIG.5

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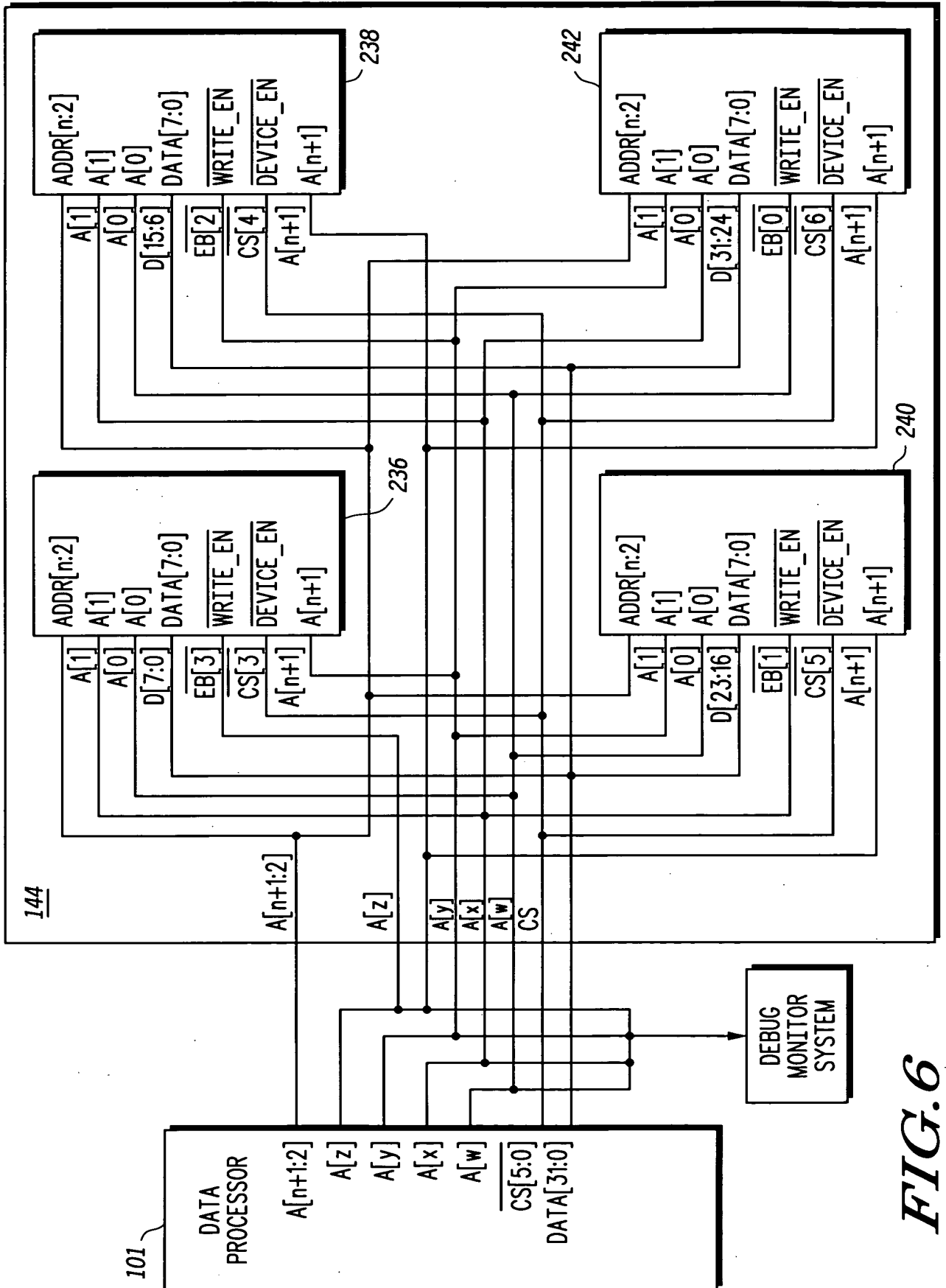


FIG. 6

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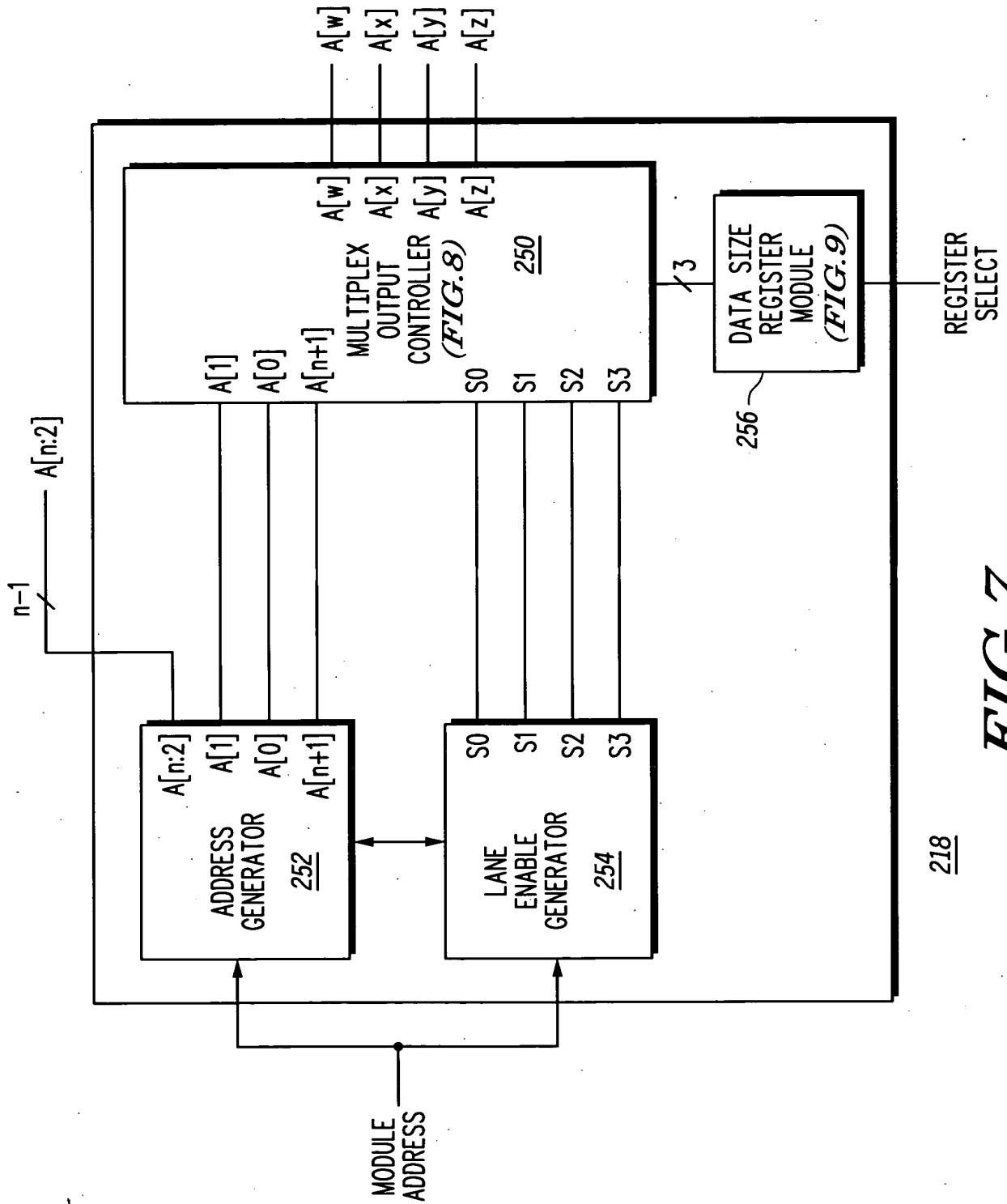


FIG. 7

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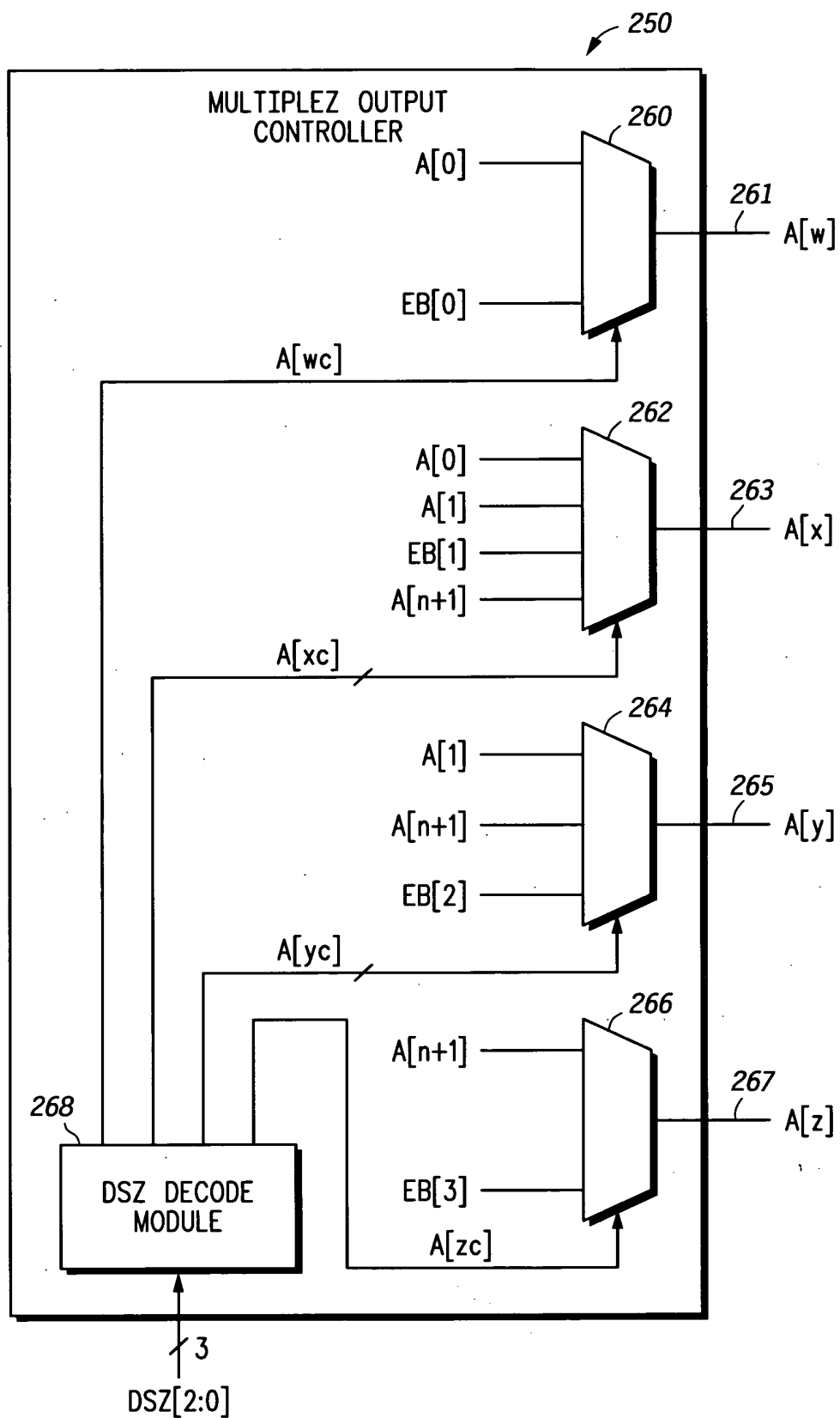


FIG. 8

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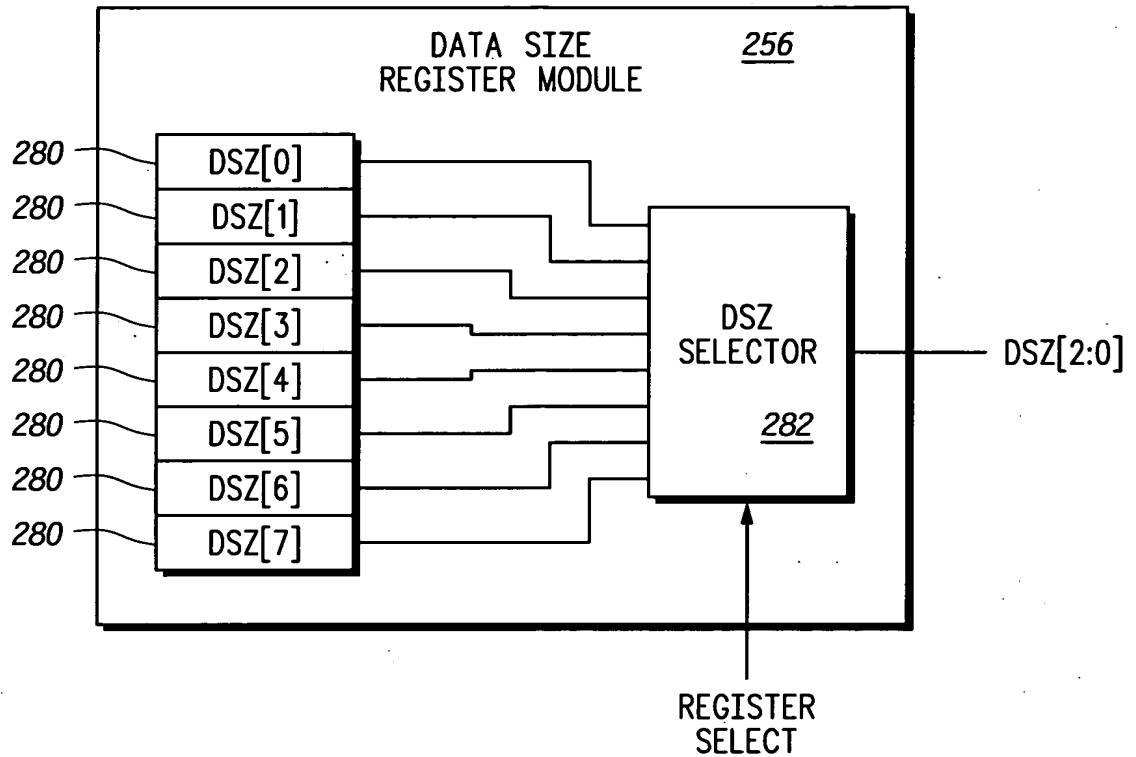


FIG.9

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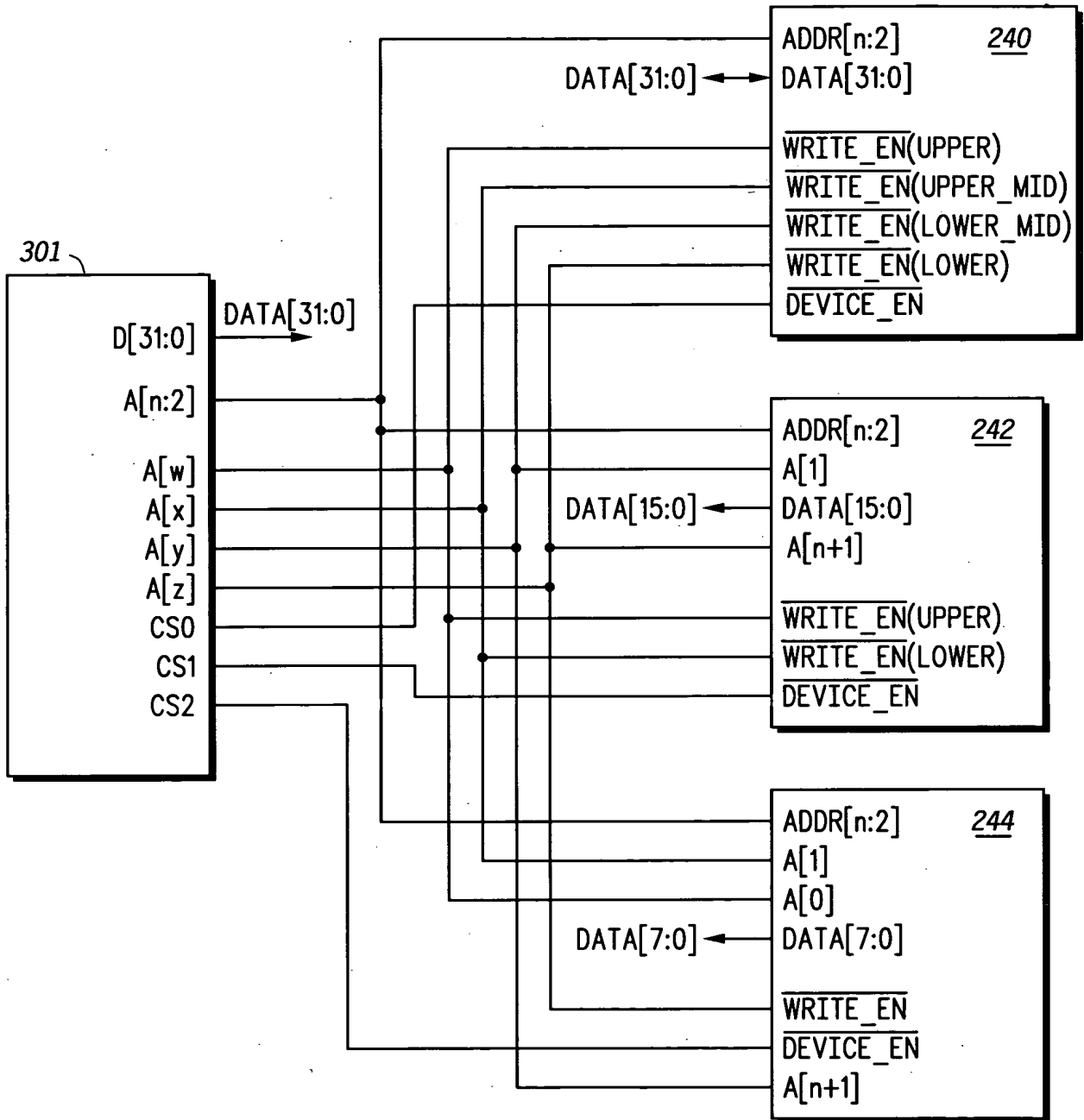


FIG. 10